IDEC Chip Design Contest

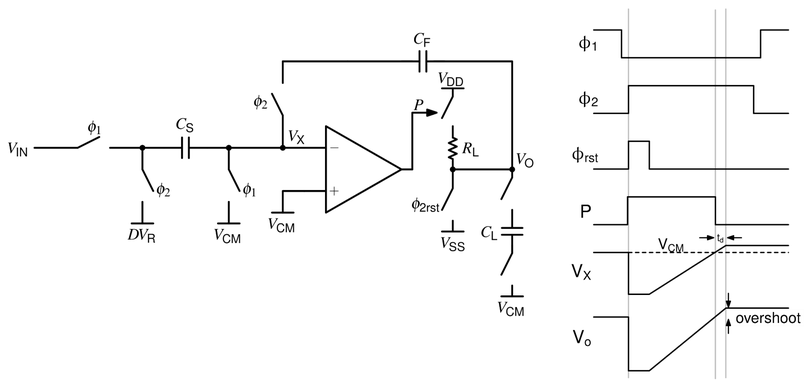
Low-Power Design of Zero-Crossing-Based Switched-Capacitor Integrator Using Non-Zero Reset Voltage

Dong-Jick Min*, Soo Hwan Kim and Jae Hoon Shim
School of Electronic and Electrical Engineering, Kyungpook National University

Introduction

- The static power of ZCBIs can be reduced by replacing OTA with a ZCD and a current source.
- However, the dynamic power may increase because of the reset phase.
- By using a non-zero reset voltage, the dynamic power consumption of ZCBIs can be reduced.

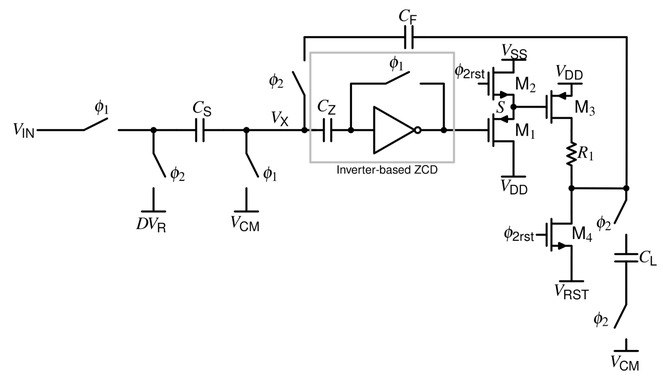
Conventional ZCBI



- The ZCD and current source replace the OTA.
- V_X should be lower than V_{CM} at the beginning of charge transfer phase (ϕ_2).
- V_X at the beginning of ϕ_2 can be expressed as

$$V_X = \frac{C_S}{C_S + C_F} DV_R - \frac{C_S}{C_S + C_F} v_{in}[n] - \frac{C_F}{C_S + C_F} v_o[n].$$

Dynamic Energy



- The energy required to charge a capacitance C_L from 0 V to $V_O[n]$ is given by

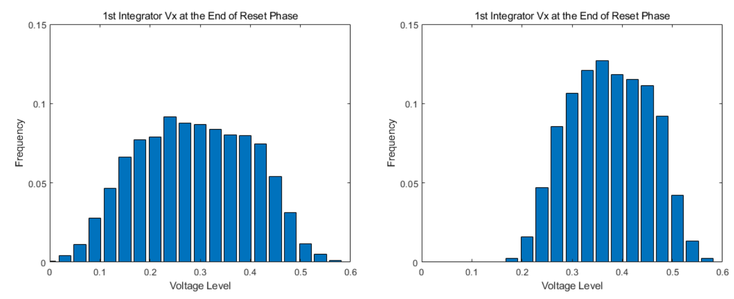
$$E_L = C_L \cdot V_{DD} \cdot V_O[n].$$

- The energy required to charge the integrator output from V_{RST} to $V_O[n]$ would be

$$E_L = C_L \cdot V_{DD} \cdot (V_O[n] - V_{RST}).$$

- If the output node is reset to non-zero voltage (V_{RST}), the dynamic power can be reduced.

Vx Histogram



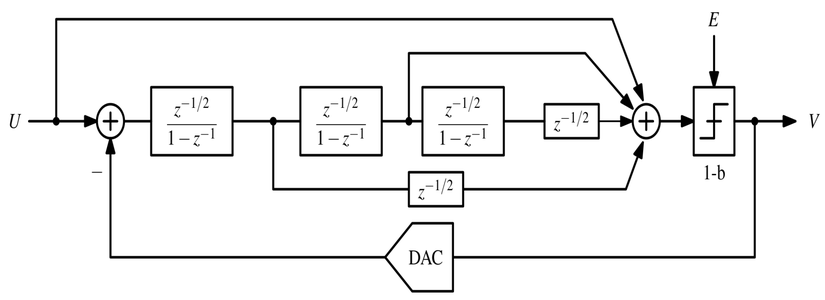
< Vx Histogram when output is reset to zero (left) or non-zero voltage (right) >

- When output node is reset to V_{RST}, V_X at the beginning of ϕ_2 is changed to

$$V_X = \frac{C_S}{C_S + C_F}(DV_R - v_i[n]) + \frac{C_F}{C_S + C_F}(V_{RST} - v_o[n]).$$

- Even with the non-zero reset voltage, V_X is always lower than the common-mode voltage(V_{CM} = 0.6 V).

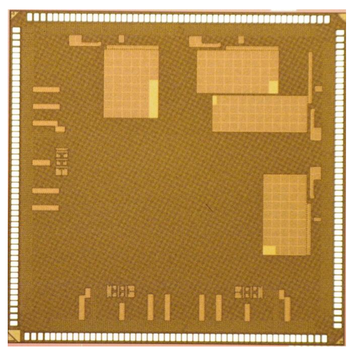
Implementation



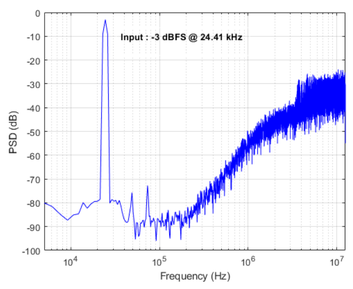
- 3rd-order Delta-Sigma Modulator.
  : Low-distortion feedforward structure.
- Half-delay and pseudo-differential integrators.

Measurement

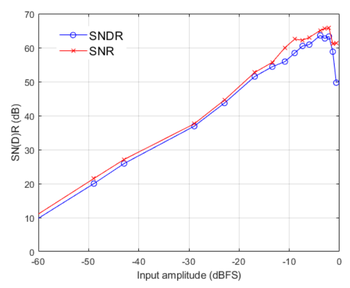
- Technology
  : 65-nm Samsung
- Core Area
  : 0.35 mm x 0.2 mm
  (0.07mm^2)



- Measurement Results



Power Spectral Density (PSD)



Input Amplitude vs. SN(D)R

Performance Summary

Type	Zero Reset	Non-Zero Reset
Technology(nm)	65	65
Supply voltage(V)	1.2	1.2
Bandwidth(kHz)	196	196
FS(MHz)	25	25
OSR	64	64
Power (uW)	360	312
Peak SNR (dB)	66.1	66.6
Peak SNDR (dB)	63.6	63.9

- SNR & SNDR are almost same when the non-zero reset voltage is applied.
- The power consumption is reduced by resetting the output node to a non-zero voltage.

Conclusion

- The measurement shows that the power consumption can be reduced by using a non-zero reset voltage while maintaining SNR/SNDR performance.

Acknowledge

- The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea.